CLAIMS

1.   A semiconductor device comprising:

a plurality of memory blocks each having memory cells;

a plurality of redundancy units for replacement of defective memory cells in the plurality of memory blocks; and

a plurality of storage circuits each configured to store a defective address assigned to a defective memory cell in the plurality of memory blocks, and also store mapping information indicative of a relationship with the redundancy units;

wherein the number of the storage circuits is smaller than the number of the redundancy units.